AN11136

Buck converter driver for SSL applications

Rev. 1 — 10 May 2012 Application note

Document information

Info	Content
Keywords	SSL2109, Buck, GreenChip, Down converter, LED controller, Topology, Retrofit SSL, LED, SSL2109, BCM, External switch
Abstract	This document describes how to design a buck converter, using the SSL2109 IC, for non-mains dimmable LED applications. Read the AN10876 for general information about buck converter applications. AN11041 describes a step-by-step design procedure for the SSL2109 family ICs.

Revision history

Rev	Date	Description
v.1	20120510	first issue

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

This application note discusses the specific design details of the SSL2109, which is a member of the SSL2108X platform, but with an external switch.

The SSL2108X platform is specifically defined to address the market of non-dimmable retrofit SSL applications. It provides a controller, with an external high-voltage switch. The platform is optimized to make cost-effective, highly efficient buck converter solutions for high-voltage LED strings or LED modules. The buck converter is one of the most used Switch Mode Power Supply (SMPS) topologies.

Information and design tools for this IC can be found on the product page on the NXP web site.

1.1 Functional description

The SSL2109 is a Multi-Chip Module (MCM) SO8 package. It can handle up to 600 V (DC) at pins HV and DRAIN. The main features for all variants are as follows (See Figure 1):

Switch-mode buck controller with power-efficient boundary conduction mode of operation with:

- No reverse recovery losses in freewheel diode
- Zero Current Switching (ZCS) for switch-on of switch
- Zero voltage or valley switching for switch-on of switch
- Smallest possible inductance value and size

Pulse Width Modulation (PWM) dimming possible

Fast transient response through cycle-by-cycle current control thus preventing:

- Overshoots and undershoots of the LED current

No binning on LED forward voltage required because of output current regulation

Internal Protections:

- Undervoltage LockOut (UVLO)
- Leading-Edge Blanking (LEB)
- OverCurrent Protection (OCP)
- Short-Winding Protection (SWP)
- Internal overtemperature
- Brownout protection
- Output short protection
- External temperature protection with single Negative Temperature Coefficient (NTC) only

See the *SSL2109 data sheet* (Ref. 2) for more information.

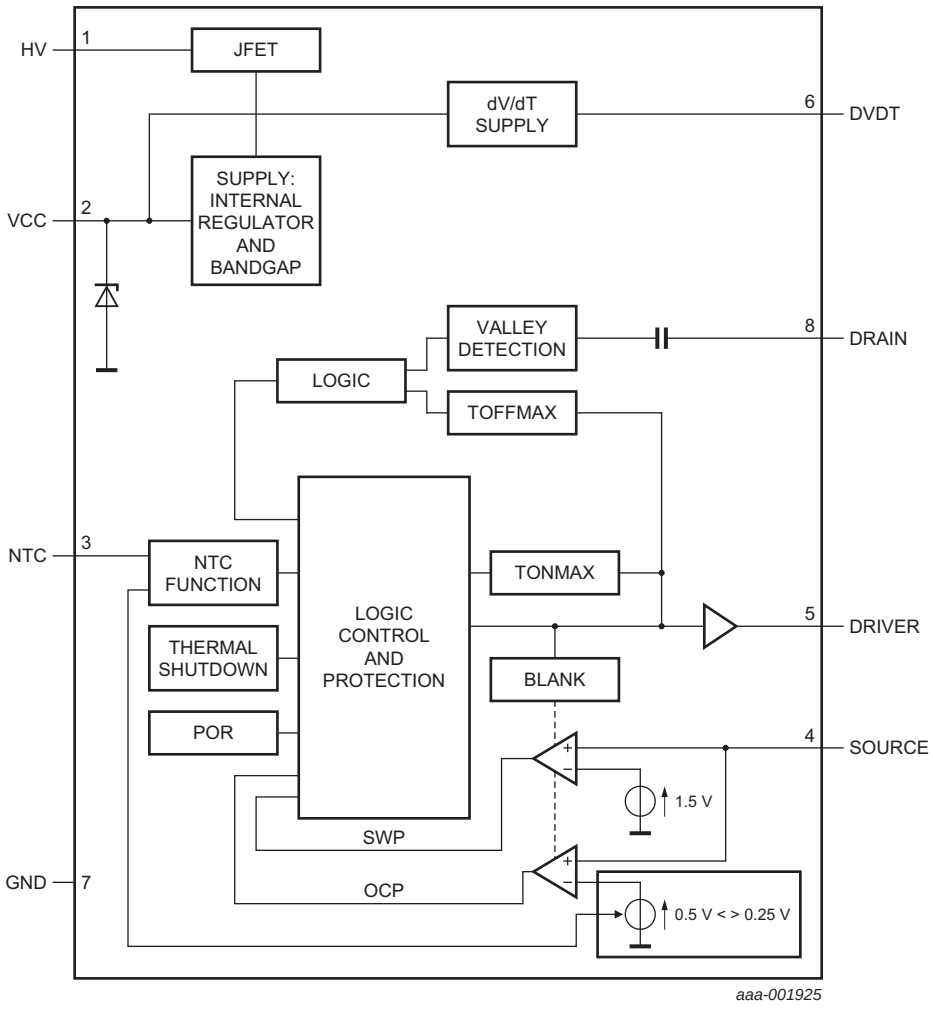


Fig 1. Block diagram SSL2109

2. Application diagram

A typical buck application for the SSL2109, driving a single LED chain, is shown in Figure 2. The mains voltage is rectified, filtered and buffered in the input section. From there, the current flows through the LED string and the inductor to pin DRAIN of the external MOSFET Q1. During switching of the external MOSFET, the amount of energy stored in L2 determines the current through the LED chain. During the primary stage when the MOSFET is ON, the current through the inductor is sensed via resistors R4/R5. When 0.5 V ($V_{th(ocp)SOURCE}$) is reached at pin SOURCE, the MOSFET is switched off.

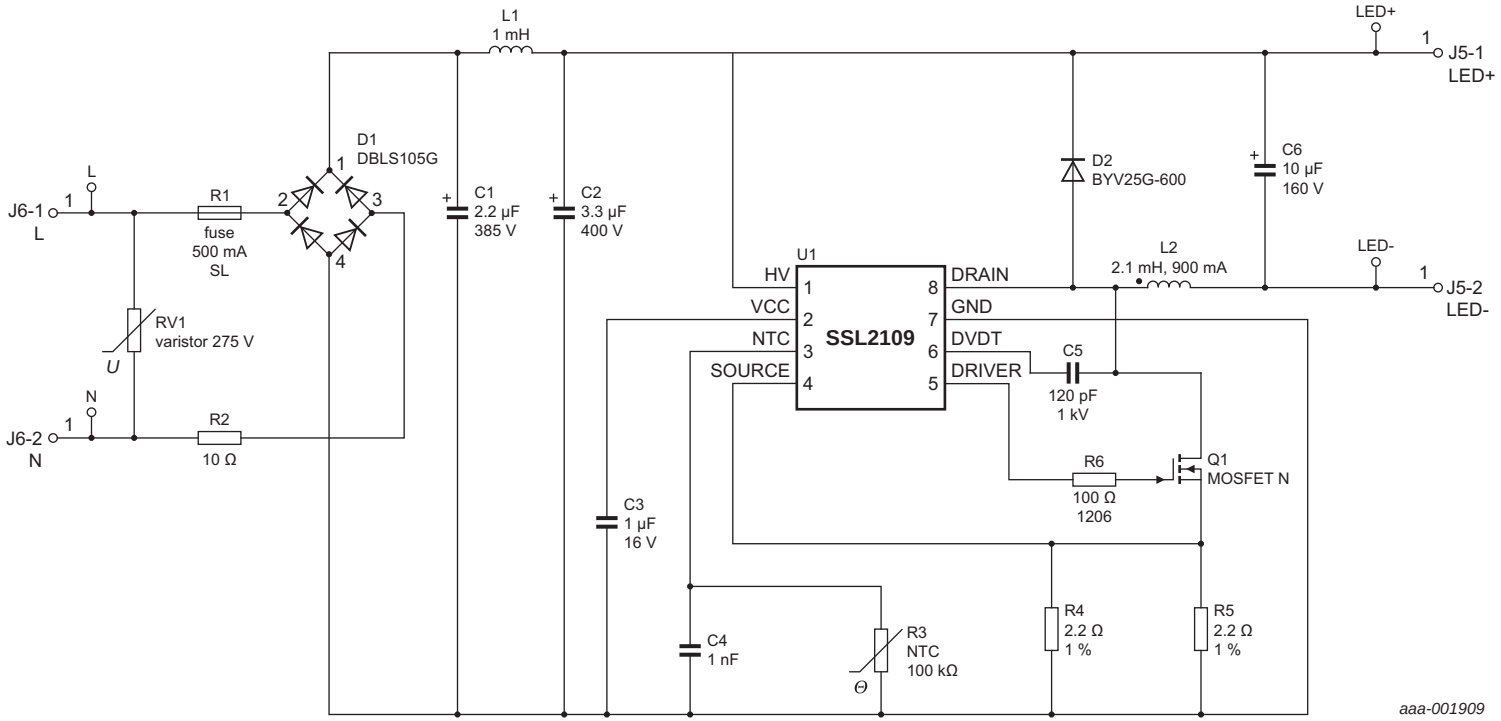


Fig 2. Application diagram SSL2109

The external MOSFET is switched on again (start of new primary stage), when the secondary stage has ended (no current through the inductor). However, this state only occurs after a valley is detected on pin DRAIN. Calculations of most components are described in the application note AN11041.

2.1 MOSFET selection

The search for a suitable MOSFET for a specific application involves minimizing the losses. Understanding how these losses depend on the switching frequency, current, duty cycle, and the switching rise and fall times is required. The MOSFET selection criteria are the position in the circuit like high side or low side. In addition, device parameters are important, such as breakdown voltage, current-carrying capability, R_{DSon}, and the R_{DSon} temperature coefficient (δ). The goal is to minimize conduction and switching losses by choosing a device with adequate thermal properties. This ensures that device selection is cost-effective and not oversized. The following method assumes steady state operation with low input voltage ripple.

Equation 1 calculates conductive losses.

Where:

- V_i = Input voltage (DC) and V_o = Output voltage (DC)

$$P_{cond} = \frac{1}{3} \times t_1 \times f \times I_{peak}^{2} \times R_{DSon} \quad \text{and} \quad t_1 = \frac{1}{f} \times \frac{V_o}{V_i} \tag{1}$$

Remark: In Equation 1, the current through the inductor over time has no fixed value, but it rises linearly in time because of the dominant series inductance. However, the peak current is fixed at switch off (see Equation 2).

Switch-off losses:

$$P_{swoff} = \frac{1}{6} \times I_{peak} \times t_{sw} \times V_{swoff} \times f \quad V_{swoff} = V_i \tag{2}$$

Capacitive Drain switching losses:

$$P_{swon} = \frac{1}{2} \times C_D \times V_{swon}^{2} \times f \quad V_{swon} = V_i - 2 \times V_o \tag{3}$$

Capacitive gate switching losses:

$$P_G = V_G^{2} \times C_{GS} \times f \tag{4}$$

C_D stands for the total capacitance between drain and GND. It includes the internal MOSFET capacitance (C_{oss}), the external DVDT capacitor, the freewheel diode capacitance and the parasitic capacitance of the inductor. The hard switching switch-on losses are negligible at a Boundary Conduction Mode (BCM) buck converter because the current is zero at switch-on. The current rises slowly due to the inductance. The temperature rise of the device is assumed linear with dissipation:

$$\Delta_T = R_\theta \times P \tag{5}$$

P stands for the dissipation inside the device. R_θ is the thermal resistance of the device with the surroundings. These equations are simple enough to allow a quick check of a given MOSFET's suitability in a specific application. However, the strong dependency of R_{DSon} on the junction temperature complicates the calculation.

$$R_{DSon} = R_{DSon\_25C} \times (1 + \delta \times \Delta_Y) \quad (6)$$

Equation 6 provides the junction-temperature rise as a function of the load current and a specific set of MOSFET parameters. The factor δ can be derived from the MOSFET data sheet by taking two points on the T_j/R_{DSon} graph. A junction temperature of about 105 °C is usually a good first cut for commercial applications.

Equation 7 is the result of combining equations 1 to 6

$$P = \frac{2 \times \frac{V_o}{V_i \times f} \times {I_{peak}}^2 \times R_{DSon\_25C} + 3 \times C_D \times (V_i - 2 \times V_o)^2 + 6 \times {V_G}^2 \times C_{GS} + I_{peak} \times t_{sw} \times V_i}{\frac{6}{f} - 2 \times \frac{V_o}{V_i \times f} \times {I_{peak}}^2 \times R_{DSon\_25C} \times \delta \times R_\theta} \quad (7)$$

Equation 7 can be rewritten to a state where maximum allowable peak current is calculated as function of all parameters:

$$I_{peak} = \frac{-b \pm \sqrt{b^2 - 4 \times a \times c}}{2 \times a} \quad (8)$$

Where:

$$a = 2 \times R_{DSon\_25C} \times \frac{V_o}{V_i} \times (1 + \delta \times R_\theta \times P) \quad (9)$$

$$b = t_{sw} \times V_i \times f \quad (10)$$

$$c = 3 \times C_D \times f \times (V_i - 2 \times V_o)^2 + 6 \times {V_G}^2 \times {C_{GS}}^2 \times f - 6 \times P \quad (11)$$

Example:

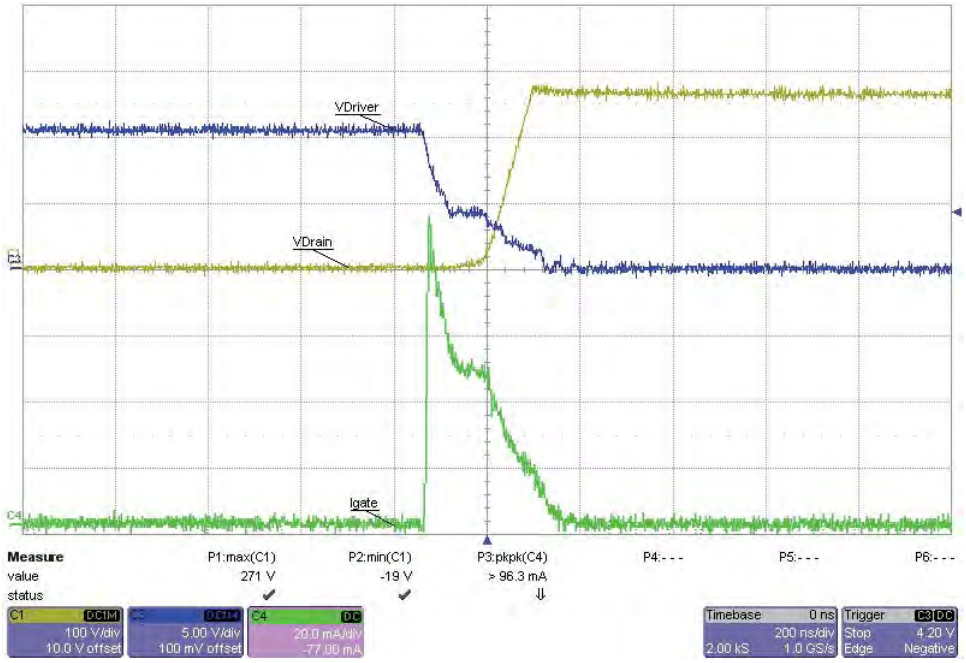
At V_i = 200 V (DC), V_o = 70 V, V_G = 10 V, R_{DSon_25C} = 1.47 Ω, f = 50 kHz, C_D = 44 pF, t_{sw} = 100 ns, C_{GS} = 11.5 pF, δ = 0.0045, R_θ = 63.
Allowable dissipation = (105 − 25) / 63 = 1.27 W. R_{DSon} = 2 Ω.

The resulting maximum current I_{peak} = 2 A.

P_{swoff} = 333 mW, P_{RDSon} = 933 mW.

2.2 Driver resistor dimensioning

R6 is a resistor mounted between pin DRIVER and the gate of Q1. It controls the peak current into pin DRIVER and the switching slope steepness of the current and voltage on the drain of Q1. See Figure 3 and Figure 4 for waveforms. Switch-on occurs at the valley of the drain voltage.



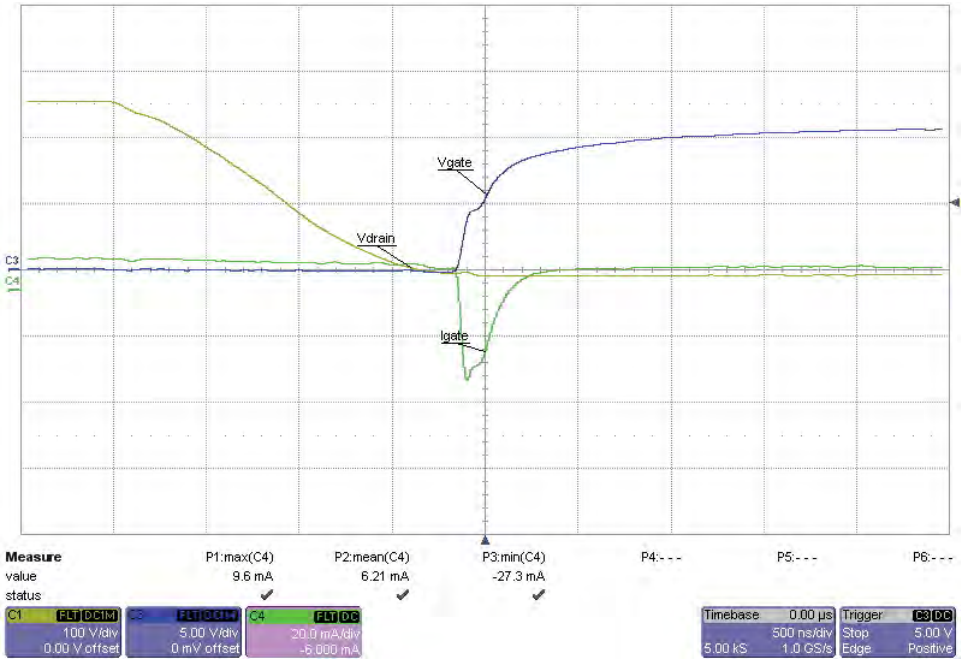
aaa-001910

(1) C1: Yellow: Voltage, DRAIN pin

(2) C3: Blue: Voltage, DRIVER pin

(3) C4: Green: Current into DRIVER pin

Fig 3. Waveforms at switch-off



(1) C1: Yellow: Voltage, DRAIN pin

(2) C3: Blue: Voltage, DRIVER pin

(3) C4: Green: Current into DRIVER pin

Fig 4. Waveforms at switch-on

The criteria that determine the value of R6 include:

- The dV/dt must not exceed a value that causes excessive voltage of the drain due to series inductance
- The gate must not rise above threshold due to voltage spikes on the drain (gate lifting)
- The current into pin DRIVER must not exceed the maximum value that this pin can handle
- The MOSFET must conduct completely before the LEB time (t_{leb}) has ended
- Maximize slope steepness (higher efficiency) while having a good resulting EMC pattern

Figure 5 shows a simplified diagram displaying the most important components that determine R6 calculation.

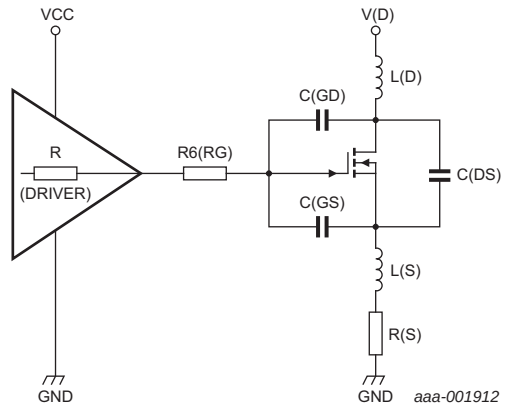


Fig 5. Driver circuit diagram

The parameters in Figure 5 are used in Equation 12 to Equation 16.

Maximum drain voltage

The turn-off switching slope results in a current change in the drain. Internal stray inductance in the MOSFET package and inductance on the PCB track generate an additional voltage on pin DRAIN. The additional voltage must not exceed the maximum drain voltage. The following equations can be applied:

Condition: $V_{D(max)} \geq V_D + V_{LC}$

Where $V_{D(max)}$ stands for the maximum permissible voltage on the MOSFET DRAIN pin and V_D the nominal operating voltage. V_{LC} is the induced voltage. The induced voltage can be calculated with Equation 12:

$$V_{LC} = \sqrt{\frac{L_D \times I_D^2}{C_{oss} + C_5}} \quad (12)$$

Example: When C_{oss} = 44 pF, C5 = 120 pF, L_D = 1 μH and I_D = 500 mA, V_{LC} = 39 V. If $V_{D(max)}$ = 400 V and V_D = 300 V, no additional measures are necessary.

For the SSL2109, most of the used external MOSFETs are avalanche rugged and withstand some excessive voltage over a short time period. For the SSL2108X, the internal MOSFETs are not avalanche rugged and have no specified safe operating area. Any excursion above the critical V_{ds} results in catastrophic breakdown. Take strict precautions to avoid overvoltage during all use cases, for example, during mains surges.

Gate lifting

As a result of fast rising voltage transients on the drain, the internal MOSFET capacitor (C_{GD}) generates a current that lifts the gate voltage. However, an unwanted opening of the switch can occur when the resulting voltage exceeds the threshold voltage of the MOSFET. This condition can destroy the MOSFET due to overcurrent or overpower.

Condition: $V_{GS} < V_{th}$

$$V_{GS} = I_{R6} \times (R6 + R_{DRIVER}) = (R6 + R_{DRIVER}) \times C_{GS} \times \frac{dV}{dt} \quad (13)$$

Example: When the switch-off time = 100 ns at 300 V, C_{GD} (C_{rss}) = 11.5 pF, dV/dt = 3 KV/µs. At V_{th} = 3.75 V, R6 + R_{DRIVER} = 108.7 Ω. The current = 34.5 mA. If R_{DRIVER} = 6 Ω, R6 must be 102 Ω or less.

This value can be checked by measuring the voltage between gate and source at closure (blue line C3 in Figure 3).

Current pin DRIVER

When pulling the gate voltage down, a current flows into pin DRIVER. This current cannot exceed the maximum permissible current.

Condition: $I_{sink(DRIVER)} < I_{R6}$

$$R6 + R_{DRIVER} = \frac{V_{o(DRIVER)max}}{I_{sink(DRIVER)}} \quad (14)$$

Example: When $V_{o(DRIVER)max}$ = 11 V and $I_{sink(DRIVER)}$ = 200 mA, then R6 + R_{DRIVER} must be larger than 55 Ω and R_{DRIVER} must be larger than 49 Ω.

Conductive before t_{leb} time-out

If there is too much delay, the device switches on after the LEB time. As a result a false peak current detection or the SWP can be activated. For this calculation, use the total gate charge Q_g.

Condition: $t_{on} < t_{leb}$

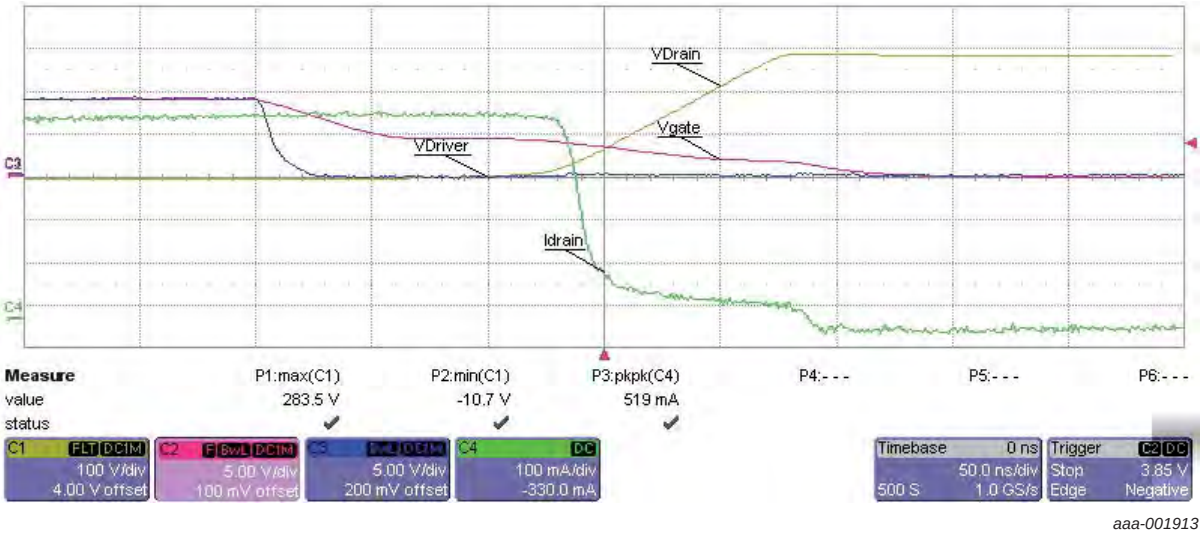
$$t_{on} = \frac{Q_G \times (R6 + R_{DRIVER})}{V_{o(DRIVER)max} - V_{th}} \rightarrow R6 < \frac{t_{leb} \times (V_{o(DRIVER)max} - V_{th})}{Q_G} - R_{DRIVER} \quad (15)$$

Example: When t_{leb} = 210 ns, $V_{o(DRIVER)max}$ = 11 V, V_{th} = 3.75 V, Q_g = 12 nC and R_{DRIVER} = 6 Ω, then R6 must be smaller than 120 Ω.

Summarizing these steps, there is a remaining bandwidth for R6 of between 49 Ω and 102 Ω (selectable).

Slope steepness versus EMC pattern

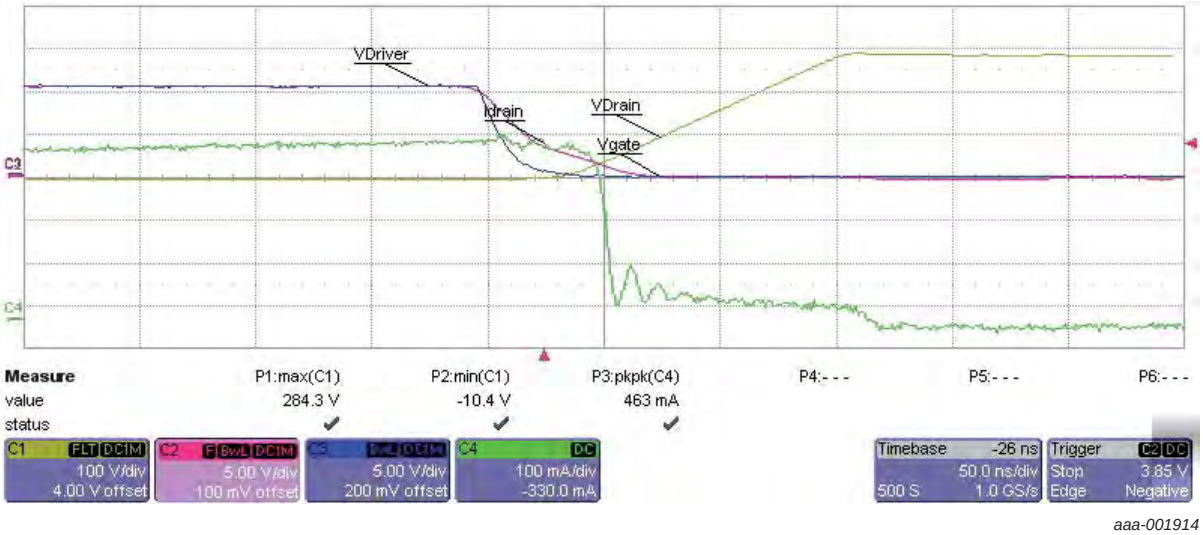
Resistor R6 controls the gate and drain voltage slope



aaa-001913

(1) C1: Yellow = Voltage DRAIN pin
(2) C2: Red = Voltage, GATE pin
(3) C3: Blue = Voltage, DRIVER pin
(4) C4: Green = Current into DRAIN pin

Fig 6. Gate signals with 100 Ω gate resistor



aaa-001914

(1) C1: Yellow = Voltage DRAIN pin
(2) C2: Red = Voltage, GATE pin
(3) C3: Blue = Voltage, DRIVER pin
(4) C4: Green = Current into DRAIN pin

Fig 7. Gate signals with 16 Ω gate resistor

A higher value for R6 reduces the steepness of the drain current slope at switch-off (C4 in Figure 6 and Figure 7). However, there is no impact on the drain voltage slope (C1). The forward transconductance of the MOSFET and the voltage slope steepness on the gate determine the current slope steepness.

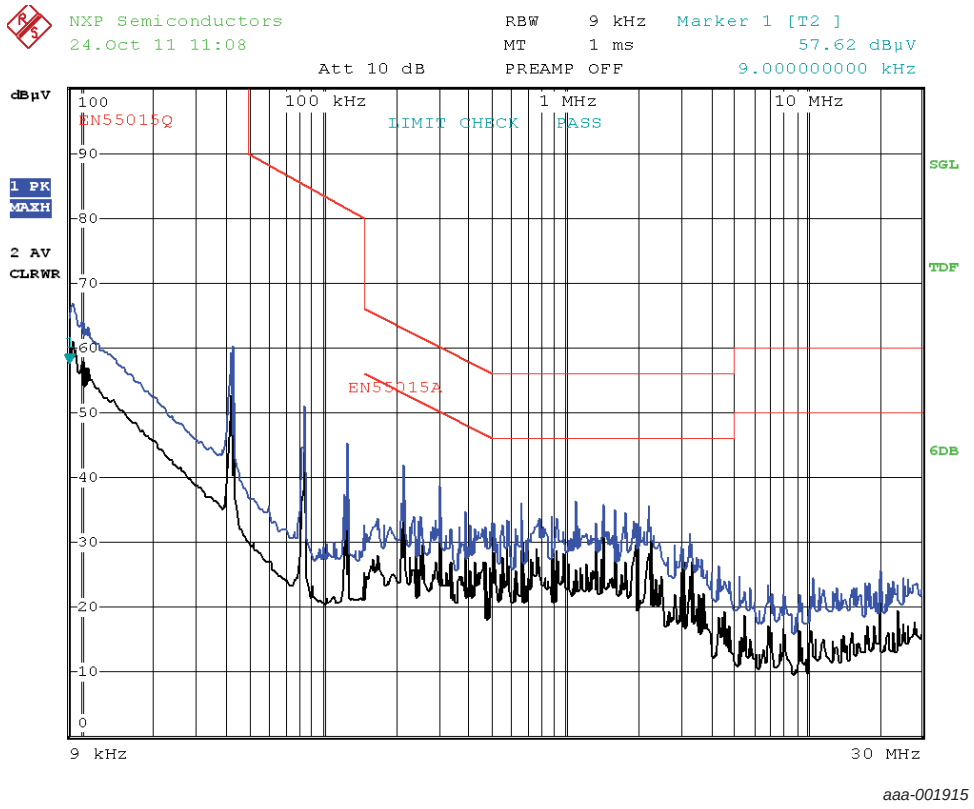


Fig 8. EMC spectrum with 100 Ω gate resistor

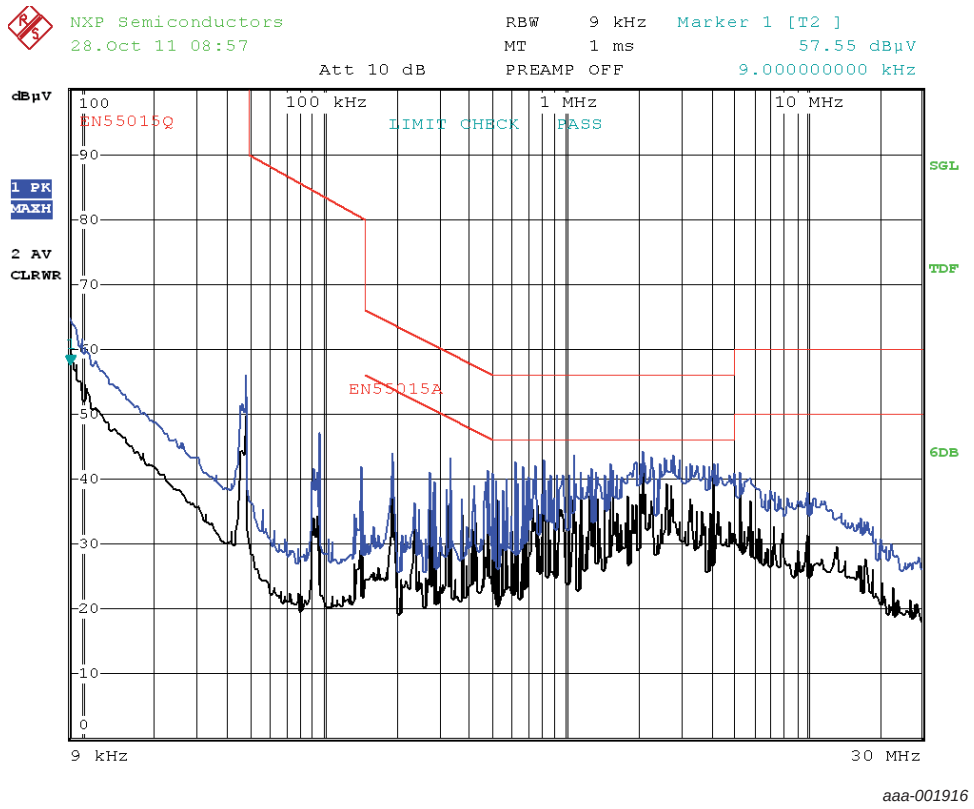


Fig 9. EMC spectrum with 16 Ω gate resistor

Equation 16 can be applied:

$$\frac{dI_D}{dt} = \frac{dV_G}{dt} \times g_{fs} = \frac{V_{th} \times g_{fs}}{C_{iss} \times (R6 + R_{DRIVER})} \rightarrow R6 = \frac{V_{th} \times g_{fs}}{\frac{dI_D}{dt} \times C_{iss}} - R_{DRIVER} \quad (16)$$

Example: When C_{iss} = 305 pF, g_{fs} = 2.2 S, V_{th} = 3.75 V, dI/dt = 0.3 A/ns and R_{driver} = 6 Ω, then R6 must be larger than 84 Ω.

Using the conditions above, the remaining selectable range for R6 is between 84 Ω and 102 Ω. A 100 Ω resistor was selected.

2.3 Gate driver losses

Driving the MOSFET gate induces losses and requires additional current for the IC VCC supply (I_{CC}). The switching frequency and the required gate charge determine the losses.

$$I_{CC} = f_{sw} \times Q_G + 500 \cdot 10^{-6} \quad (17)$$

$$I_{g(rms)} = f_{sw} \times Q_G \quad (18)$$

The energy required is:

$$P_G = V_G \times f_{sw} \times Q_G \quad (19)$$

If we take the model of Figure 5, this power is distributed over R_{DRIVER} and R6 according to the ratio between these resistors:

$$P_{RDRIVER} = \frac{R_{DRIVER}}{R_{DRIVER} + R6} \times P_G \quad (20)$$

$$P_{R6} = \frac{R6}{R6 + R_{DRIVER}} \times P_G \quad (21)$$

Example: When Q_G = 11.7 nC, f = 50 kHz, V_G = 11 V, R_{DRIVER} = 6 Ω, R6 = 100 Ω, then I_G = 585 μA, P_G = 6.44 mW, P_{R6} = 6.07 mW and $P_{RDRIVER}$ = 0.37 mW.

In the examples, at normal loads, the dissipation inside the package is small. However, it is possible to load the output excessively, causing the IC to enter overtemperature protection. Thus, it is recommended not to load the gate driver with more than 110 nC (10 nF).

2.4 VCC supply via DVDT pin

This topic is explained in the application note *"SSL2108x driver for SSL applications" (AN11041), section 4.7.1*.

3. Output open protection

This chapter describes two methods to add open output protection to the SSL2108X series. Output open is when no load is attached or when there is a defect in the LED load resulting in an open condition. This situation does not damage the IC, but the output voltage increases to a level just under the rectified buffer voltage level. If the rated voltage for capacitor C6 is incorrect, C6 can be damaged. Furthermore, there can be an excessive discharge current through the LED load when it is attached while the converter is on (hot-plugging). The output open detection can easily be added to prevent excessive discharge current. Two protection methods can be used:

1. Using the ICs output short detection. When there is overvoltage, the output can be shorted below a level where valley is not detected anymore. As a result, the IC enters latched protection after a certain time ($t_{det(sc)}$). Figure 10, shows a possible implementation.

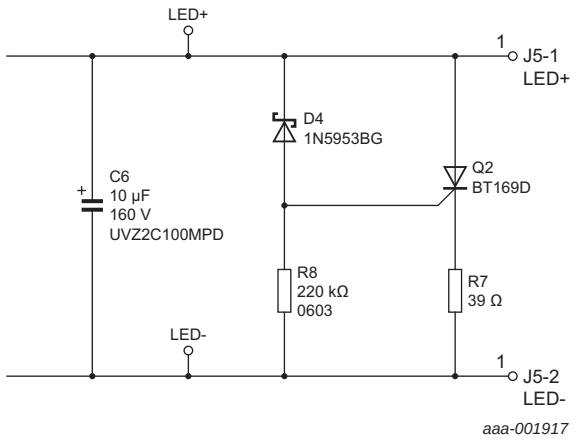


Fig 10. Output open protection using short detection of the IC

2. Pulling the NTC pin low causes entry into latched protection. A level shifter is therefore required. Figure 11 shows a possible implementation.

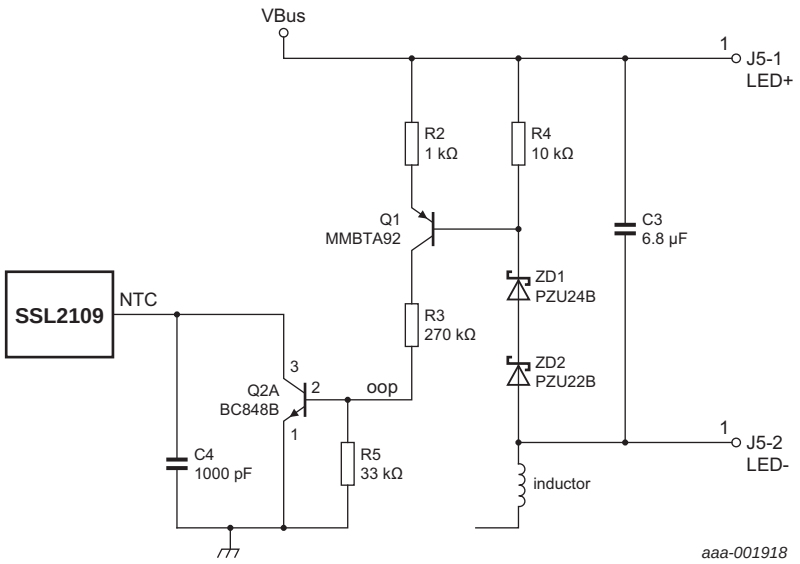
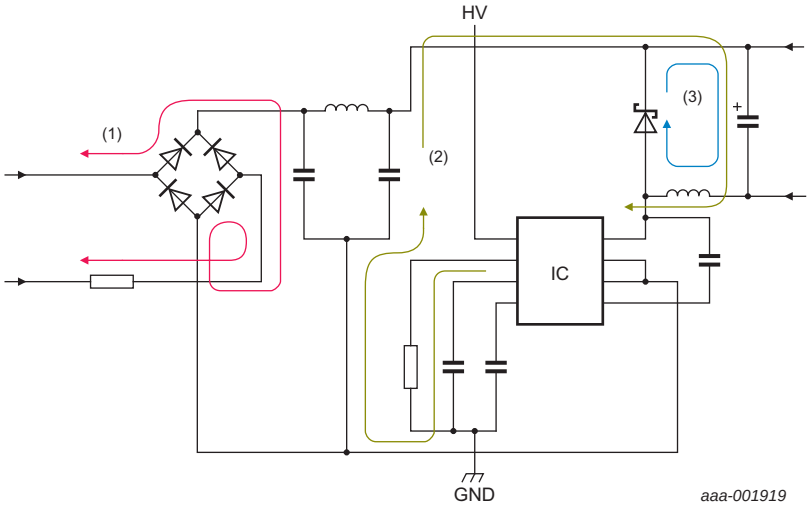


Fig 11. Output open protection using the NTC pin

In this schematic, Zener diodes ZD1 and ZD2 start to conduct if the output voltage exceeds a threshold of about 47 V. The resulting current out of the base of Q1 causes the voltage on node OOP to rise. This results in pulling the NTC pin voltage below 0.2 V with Q2A. This condition disables the converter. R2 is added to limit current though Q1-ZD1-ZD2.

4. EMC considerations

General information on layout and ElectroMagnetic Compatibility (EMC) is available in *application note AN10912*. For the SSL2108X series, pay particular attention to the ground circuit layout. See *AN10912 chapter 5.6.3* about grounding techniques. Use star configuration grounding to avoid false triggering of SWP. This condition remains true if the drop is long enough (> 32 μs). As an illustration, a faulty layout (see Figure 13) is compared with a good layout (see Figure 14).



(1) Surge current
(2) t_{on} current
(3) t_{off} current

Fig 12. Schematic with current loops

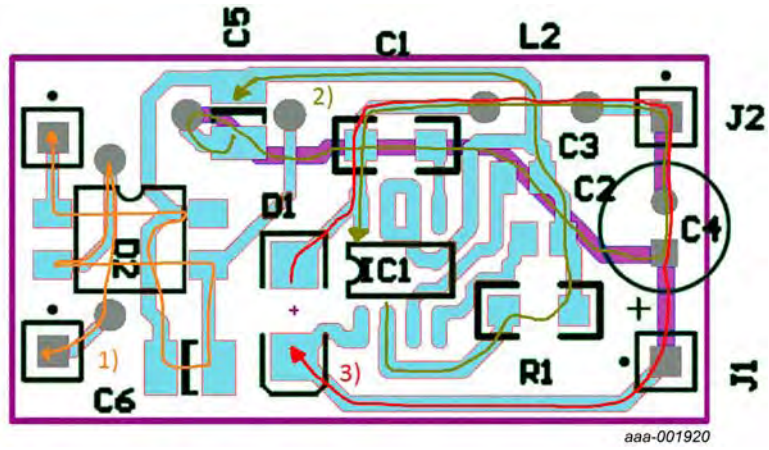


Fig 13. Faulty layout

In Figure 12, an SSL21083 IC is used. The following points are incorrect:

1. L1 (input common-mode choke) has wrong orientation increasing coupling over the Pi filter. The solution is to rotate L1 180 degrees.
2. D1 (freewheel diode) is placed opposite the circuit. This creates a current loop that encompasses a large part of the PCB. The circuit is equivalent to D2/L2/C6 in Figure 2. As a result, switching spike voltages are induced in all traces within this area. The solution is to move D1 closer to C4.
3. C5 (decoupling capacitor) is placed at a distance of converter currents, thus increasing the loop size.
4. The current flowing due to the mains switch circuit must not coincide with small circuit GND traces. Solution: Separate power tracks from signal tracks and make one combined star grounding point at IC GND.
5. The value of C6 is not sufficient for surge or lighting protection (not EMC related).

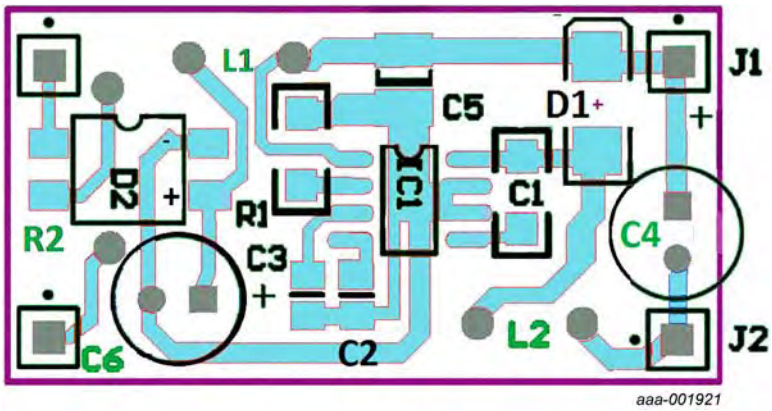


Fig 14. Good layout

5. Abbreviations

Table 1. Abbreviations

Acronym	Description
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
EMC	Electro Magnetic Compatibility
GND	Ground
IC	Integrated Circuit
LEB	Leading-Edge Blanking
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTC	Negative Temperature Coefficient
OCP	OverCurrent Protection
PCB	Printed-Circuit Board
PWM	Pulse Width Modulation
RMS	Root Mean Square
SMPS	Switch Mode Power Supply
SSL	Solid-State Lighting
SWP	Short Winding Protection
ZCS	Zero Current Switching

6. References

[1] **SSL2108X —** Data sheet: Drivers for LED lighting

[2] **AN10876 —** Application Note: Buck converter for SSL applications

[3] **UM10512 —** User manual: Buck converter driver for SSL applications

[4] **SSL2109 —** Data sheet: Buck converter driver for SSL applications

7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

8. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 May 2012
Document identifier: AN11136